EC835

USN

NEW SCHEME

Eighth Semester B.E. Degree Examination, May 2007
Electronics and Communication Engineering
Embedded System Design

Time: 3 hrs.] [Max. Marks:100

Note : *Answer any FIVE full questions.*

1 a. Explain the various metrics that need to be optimized while designing an embedded system. (08 Marks)

b. Explain the three main processor technologies that can be used with embedded system. Also highlight the benefits of each. (06 Marks)

c. Explain how the top-down design process improves the productivity. (06 Marks)

2 a. Explain the various steps involved in designing a custom single-purpose processor. (06 Marks)

b. Explain the concept of 'data path' in the embedded systems. (04 Marks)

c. Design a single-purpose processor that outputs Fibonacci numbers upto n. Start with a function computing the desired result, translate it into a state diagram and sketch a probable datapath. (10 Marks)

3 a. Explain the various events that take place when a processor executes an instruction. Explain how does pipelining improves the execution speed. (08 Marks)

b. Explain the various addressing modes that are commonly used by processors. (04 Marks)

c. Explain the steps involved in designing a general-purpose processor. (08 Marks)

4 a. Explain how UART is used for communication highlighting the advantages of UART. (06 Marks)

b. Schematically explain how a PWM helps in controlling the speed of DC motor. (06 Marks)

c. Highlight the advantages of using data in digital form over its analog form. Explain the working of successive approximation type of analog to digital converter. (08 Marks)

5 a. Explain the various types of RAM highlight the features of each. (06 Marks)

b. What is cache memory? Explain its need and how it helps in improving the execution speed. (06 Marks)

c. With a neat diagram explain the advanced RAM architecture. Also explain how this is extended to improve the performance through synchronous DRAM. (08 Marks)

Contd... 2

6 a. What is multi-level bus architecture? Explain its need and also the reasons to improve the processor performance by this architecture. (06 Marks)

b. Explain the reasons that make the serial communication more preferred than the parallel communication systems. (06 Marks)

c. Explain how I^2C bus structure in peripherals to communicate with the processor. (08 Marks)

7 a. Explain the need for interrupts in processing systems. Also explain the various events that take place when a processor is interrupted. (06 Marks)

b. Explain the problems associated with interrupts that deals with the shared-data. Also suggest solutions to solve these problems. (08 Marks)

c. What is interrupt latency? Explain the factors affecting it. (06 Marks)

8 a. Explain the reasons why the systems with the conventional operating system fail to respond to the real time problems. Also explain how these are taken care in RTOS. (06 Marks)

b. Explain the concept of semaphores. How these help us in solving the shared – data problem in embedded systems? (08 Marks)

c. Differentiate between hard and soft RTOS highlighting the advantages and disadvantages of each. (06 Marks)

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EC83

Eighth Semester B.E. Degree Examination, May/June 08
Embedded System Design

Time: 3 hrs. Max. Marks:10

Note : *Answer any FIVE full questions.*

1 a. Differentiate between the following
   i) Single purpose and general purpose processors.
   ii) Full custom IC and PLD technologies (08 Marks)

b. Explain the following terms
   i) Characteristics of an embedded system
   ii) Ideal top – down design process. (06 Marks)

c. Define time – to – market and NRE cost metrics. The lifetime of a product is 60 weeks and if the product is delayed by 7 weeks, determine the percentage revenue loss. Determine the per – product cost if the NRE cost is Rs 4,00,000 and unit cost is Rs 8000 and the company produces 5000 units of that product. (06 Marks)

2 a. Write s simple algorithm for finding the GCD of two integer numbers. Write the FSMD for this algorithm and explain how it can be optimized and write the optimized FSMD and its advantages. (08 Marks)

b. Explain the following 3 addressing modes with an example from any processor
   i) Register indirect
   ii) Relative addressing
   iii) Direct (06 Marks)

3 a. Explain the following terms
   i) Superscalar architecture
   ii) Linker
   iii) Dhrystone Benchmark
   iv) Cross compiler (08 Marks)

b. Differentiate between
   i) Harvard and Princeton architectures
   ii) Microcontrollers and DSPs. (06 Marks)

c. Explain pipelining. If 6000 instructions are to be executed using a 4 stage pipelined processor at a clock frequency of 12 MHz, determine the speedup of the pipelined processor when compared to a non – pipelined processor. (06 Marks)

4 a. Describe the working of PWM with necessary diagrams and explain how it can be used in the speed control of DC motor. (08 Marks)

b. What is a WDT and what is its use? A 16 bit timer operates at a clock frequency of 20 MHz. Determine the resolution and range of this timer. If a ÷ 4 – prescaler is also used what is the range and resolution of this design? (06 Marks)

c. The analog input range for an 8 bit ADC is from –2.5 V to + 7.5 V. Determine the resolution of ADC and digital output in hexadecimal when the input voltage is 1.2 V. Trace successive approximation steps and show the binary output of the ADC. (06 Marks)

5 a. Compare the following
   i) SRAM and DRAM
   ii) Direct mapped and fully associative cache memory designs. (08 Mar
   b. Explain the following terms in brief
   i) Flash memory
   ii) NVRAM
   iii) IrDA (06 Mar
   c. Compose 1k × 8 ROMs for the design of a 2 k × 16ROM. Write a block diagram showi the connections and the memory map. Determine the average memory access time, if t cache miss ratio is 0.2, cache access requires 2 cycles and main memory access requires cycles when the clock frequency is 20 MHz. (06 Mar

6 a. Explain shared data problem with an example show how interrupt facility can be used f solving this problem. (08 Mar
   b. Compare i) CAN Bus and PCI Bus ii) Serial and Parallel communication. (06 Mar
   c. Consider three processes with high, medium and low priorities respectively. The executi time values of these three processes be 100μ sec, 200μ sec and 300μ sec respectively. T minimum interrupts latency of the system be 150μ sec. Let the deadline of the low prior process be 600μ sec. Is it possible for the low priority process to execute before t deadline if the other two interrupts also occur or only medium priority process interrup it? Determine the worst case Interrupt latency values for both the cases. (06 Mark

7 a. Describe RR with interrupts with an algorithm. Mention a practical application for t same. (08 Mark
   b. Explain RTOS architecture with an algorithm. (06 Mark
   c. Compare the characteristics of the four software architectures for scheduling. (06 Mark

8 a. Write a major difference for the following topics
   i) Queues and Mailboxes
   ii) Ready and Running states
   iii) Encapsulating semaphores and encapsulating queues
   iv) Saving memory space and saving power. (08 Mark
   b. What are semaphores? Explain the structure and use of binary semaphores for da protection. (06 Mark
   c. Explain the 2 rules that the interrupt routines in a RTOS must follow. (06 Mark

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2002 SCHEME

USN | | | | | | | | | |

EC835

Eighth Semester B.E. Degree Examination, June-July 2009
Embedded System Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Derive the equation for percentage revenue loss for any market rise angle θ. A product was delayed by 4 weeks in releasing to market. The peak revenue for the product for on-time entry to market would occur after 20 weeks for a market rise angle of 45^0. Determine the percentage revenue loss. (08 Marks)

b. Compare GPP, SPP and ASSP along with their block diagrams and any two differences. (06 Marks)

c. Given the following details, draw the graphs of total cost Vs volume and per product cost Vs volume. Make a table for volumes 400, 800, 1200, 1600, 2000 and 2400 for all the three technologies.

	Technology A	Technology B	Technology C
NRE cost	$ 2,000	$ 30,000	$100,000
Unit cost	$ 100	$ 30	$ 2

(06 Marks)

2 a. Write an algorithm for GCD with more time complexity and write the FSMD and also determine the total number of steps required for GCD (42, 8) in this case. (08 Marks)

b. Explain pipelining for instruction execution with 5 stages. Determine the speed up, if 200 instructions are executed at a clock frequency of 10 MHz in this pipelined processor. (06 Marks)

c. Explain the terms : Dhrystone Benchmark, Linker and Moore's law. (06 Marks)

3 a. Explain the working of stepper motor using a deriver. (08 Marks)

b. Describe register, relative and direct addressing modes in a processor with an example for each. (06 Marks)

c. Determine the range and resolution of a 16 bit timer which operates at a clock frequency of 10 MHz and generates an overflow signal when it reaches FFFF. Calculate the terminal count value for measuring a 3 msec time interval. What is the minimum division needed in a prescaler for measuring 100 msec? (06 Marks)

4 a. The analog input range for an 8 bit ADC is – 5V to + 5V. Determine the resolution of this

b. ADC and also the digital output in binary when the input is – 2V using formula. Also trace the successive approximation steps for verification. Write it in a tabular form with necessary columns. (08 Marks)

Describe the working of a PWM unit with a circuit and waveforms. (06 Marks)

Explain the features of flash memory, SRAM and OTP ROM. (06 Marks)

5 a. Describe set associative cache mapping technique. What are its merits and demerits? (08 Marks)

b. Compose a 4 K × 32 bit ROM using a required number of 2 K × 8 bit ROMs. Show the connection diagram and write the memory map. (06 Marks)

c. Write the features of CAN bus, PCI bus and Bluetooth protocol. (06 Marks)

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6 a. Describe shared data problem with an example. Show how disable/ enable interrupt c used for solving this problem. (08 M

b. Explain interrupt handling procedure, context switching and critical section. (06 M

c. Let the minimum interrupt latency in a system be 100 µsec and context switching ti negligible. The execution time for high, medium and law priority processes be 200 400 µsec and 600 µsec respectively. The deadline for the low priority process be 1000 Is it possible for the low priority process to complete its execution if –
i) both high and medium processes interrupt it and ii) only high priority process interru Write timing diagrams for both the cases and indicate worst case interrupt latency and time. (06 M

7 a. Describe round robin architecture for digital multi-meter example. (08 M

b. Explain function queue scheduling. (06 M

c. Describe the function of a scheduler with a task state transition diagram. (06 M

8 a. Describe the use of take semaphore ( ) and release semaphore ( ) with an example. (08 M

b. Explain any 6 problems with semaphores. (06 M

c. Describe the use of message queues. (06 M

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2002 SCHEME

USN | | | | | | | | | | |

EC835

Eighth Semester B.E. Degree Examination, Dec.09/Jan.10
Embedded System Design

Time: 3 hrs. Max. Marks:100

Note: 1. ***Answer any FIVE full questions.***
2. ***Missing data may be suitably assumed.***

1 a. Define embedded system. What are the characteristics of an embedded system? **(10 Marks)**
b. What is Design metric? What are the common design metrics that a design engineer should consider? Explain each design metric briefly. **(10 Marks)**

2 a. Derive a formula to measure the percentage revenue loss due to delayed entry of the product to the market. Determine the percentage revenue loss of the product whose lifetime = 52 weeks, delayed entry = 4 weeks. **(10 Marks)**
b. Write an FSMD for GCD algorithm. Optimize the algorithm and FSMD. **(10 Marks)**

3 a. With a neat diagram, explain the functioning of a watch dog timer. Discuss the usage of watch dog timers. Write a Pseudo code for an ATM machine to demonstrate the usage of watch dog timer. **(10 Marks)**
b. What is memory hierarchy? Discuss three cache mapping techniques with their merits and demerits. **(10 Marks)**

4 a. Discuss the merits of multilevel bus architectures. With a neat diagram explain the functioning of two level bus architecture. **(10 Marks)**
b. Write a short notes on: i) CAN ii) USB iii) IEEE 802.11 iv) Blue tooth. **(10 Marks)**

5 a. Explain with a pseudo code, the classic shared data problem associated with an interrupt routine and a main program. **(10 Marks)**
b. Rewrite the pseudo code resolving the shared data problem using interrupt calls and estimate the interrupt latency. Discuss the factors that affect interrupt latency. **(10 Marks)**

6 a. Explain the characteristics of four software architectures suggested for embedded system software design. Highlight the advantages of RTOS architecture. **(10 Marks)**
b. Suggest a suitable architecture to design a digital multimeter. Implement the same with a pseudo code. **(10 Marks)**

7 a. Define reentrant function. Explain the three rules that decide the function is reentrant. How semaphores help make a function reentrant? Explain with an example. **(10 Marks)**
b. Highlight the four problems associated with semaphore usage. Explain the problem of priority inversion, and how it can be solved. **(10 Marks)**

8 a. Discuss briefly with an example, two rules that the interrupt routine should follow in an RTOS environment. **(10 Marks)**
b. Discuss the basic design considerations while designing embedded systems using RTOS. **(10 Marks)**

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Important Note: 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

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06EC82

Eighth Semester B.E. Degree Examination, May/June 2010
Embedded System Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Mention the characteristics and briefly list the design metrics of an embedded system. **(08 Marks)**

b. Determine the percentage of revenue loss if the products life time is 86 weeks and the delay in the market is 8 weeks. Derive the formula used for this calculation. **(06 Marks)**

c. Explain how the top-down design process improves the productivity. **(06 Marks)**

2 a. Briefly explain the purpose of the data path and controller in a single purpose processor. **(06 Marks)**

b. Write an efficient algorithm for finding the GCD of two integer numbers. Also explain how the FSMD for this can be optimized. **(08 Marks)**

c. Explain various addressing modes that are commonly used by processors, with an example. **(06 Marks)**

3 a. Explain how UART is used for communication. List its advantages. **(08 Marks)**

b. What is a watch dog timer? List its uses. A 16 bit timer operates at a clock frequency of 12 MHz. Determine the resolution and range of this timer. **(06 Marks)**

c. The analog input range for a 8-bit ADC is from -2.5V to 8.5V. Determine the resolution of ADC and digital output in hexadecimal, when the input voltage is 1.2V. Trace successive approximation steps and show the binary output of the ADC. **(06 Marks)**

4 a. What is memory hierarchy? How does the cache operate? Discuss the cache mapping techniques. List their merits and demerits. **(10 Marks)**

b. Briefly explain OTPROM, EEPROM, RDRAM and FPM DRAM. **(10 Marks)**

PART – B

5 a. Explain the need for interrupts in processors and mention briefly the various events that take place when a processor is interrupted. **(10 Marks)**

b. Explain the problems of shared-data interrupts and suggest the solution to solve the problems. **(10 Marks)**

6 a. Explain with an example, how the Round-Robin architecture works. What is its limitation? **(12 Marks)**

b. List the characteristics of four software architectures available for building embedded software. **(08 Marks)**

7 a. Mention the two rules of interrupt routines in an RTOS environment. With an example, briefly explain, what happens when each rule is violated. **(15 Marks)**

b. Describe the use of message queues. **(05 Marks)**

8 a. What is meant by encapsulating the semaphores? Bring out the need for it. **(08 Marks)**

b. Explain any six problems of semaphores. **(06 Marks)**

c. Explain the methods to solve memory space and methods to save power. **(06 Marks)**

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